



Reliability Report

Report Title: LTC3306 in WLCSP New Product Qualification
Report Number: 17072
Revision: A
Date: 31 January 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the LTC3306 product in a 6-WLCSP package. The LTC3306 is a 5V, 1.5A synchronous buck regulator.

Table 1: LTC3306 Product Characteristics

Die/Fab

Die Id	3306
Die Size (mm)	1.06 x 1.67
Wafer Fabrication Site	TSMC Fab 8
Wafer Fabrication Process	0.25µm BCDMOS
Approximate Transistor Count	14,712
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly

Package	6-WLCSP
Operating Temperature Range	-40°C ≤ TA ≤ 125°C
Bump Pitch (mm)	0.50
Bump Diameter (mm)	0.30
Bumping Foundry	AET (ASE)
RDL Layers	2
RDL Composition	Ti(0.1)/Cu(0.2)/Cu(5)
RDL Repassivation	Polyimide (7.5) / Polyimide (7.5)
Under Bump Metallization	Ti(0.1)/Cu(0.2)/Cu(8.6)
Bumping Process	Solder Bump over RDL
Bump Composition	95.5Sn_4.0Ag_0.5Cu
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 and 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: WLCSP at ASE (AET) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	LTC3306	Q17072.1HTS	45	0
			LTC3315	Q16993.1HTS	45	0
			LTC3307A	Q16433.2HTS	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) ¹	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264 Hours	LTC3306	Q17072.1BHAST	77	0
			LTC3306	Q17072.1	77	0
		130C 85%RH 33.3 psia, Biased, 96 Hours	LTC3315	Q16993.1BHAST	77	0
			LTC3315	Q16993.2PC.BHAST	77	0
			LTC3307A	Q16433.1BHAST	77	0
				Q16433.3BHAST	77	0
Temperature Cycling (TC)	JESD22-A104	-40°C/+125°C, 1 Cycles/Hour, 2,000 Cycles	LTC3306	Q17072.1TC	77	0
				Q17072.2TC	77	0
			LTC3315	Q16993.1TC	77	0
				Q16993.2TC	77	0
			LTC3307A	Q16433.1TC	77	0
				Q16433.2TC	77	0
Unbiased HAST (UHST) ¹	JESD22-A118	110C 85%RH 17.7 psia, 264 Hours	LTC3306	Q17072.1UHAST	77	0
			LTC3306	Q17072.2UHAST	77	0
		130C 85%RH 33.3 psia, 96 Hours	LTC3315	Q16993.1UHAST	77	0
				Q16993.2UHAST	77	0
			LTC3307A	Q16433.1UHAST	77	0
				Q16433.3UHAST	77	0

¹ These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 3: 0.25µm BCDMOS at TSMC Fab-8A Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	LTC3306	Q17072.1HTS	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) ¹	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264 Hours	LTC3306	Q17072.1BHAST	77	0
		130C 85%RH 33.3 psia, Biased, 96 Hours	LTC3306	Q17072.1	77	0
	LTC3315		Q16993.1BHAST	77	0	
	LTC3307A		Q16993.2PC.BHAST	77	0	
			Q16433.1BHAST	77	0	
	LTC3310S		Q16433.3BHAST	77	0	
			971845.1	77	0	
	High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125°C, Biased, 1,000 Hours	LTC3306	Q17072.1HTOL	77
+150°C, 1000 Hours			LTC3310S	Q17072.2HTOL	77	0
		971845.1		77	0	
		LTC3315	971846.1	77	0	
			971847.1	77	0	
Early Life Failure Rate (ELFR)		JESD22-A108 JESD74	+150°C, 48 Hours	LTC3310S	968845.1	77
	LTC3310S	971845.1	800	0		
		971846.1	800	0		
			LTC3310S	971847.1	800	0

¹ These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on [Analog Devices' web site](#).

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 4. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on [Analog Devices' web site](#)).

Table 4: LTC3306 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	6-WLCSP	JS-002	1Ω, Cpkg	±1250V	NA	C3
HBM	6-WLCSP	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	NA	3A

Latch-Up Test Results

Six samples of the LTC3306 were latch-up tested at $T_A=125^{\circ}\text{C}$ per JEDEC Standard JESD78, Class I. Pre- and post-stress electrical test was performed at room temperature. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	+6.0V

Approvals

Reliability Engineer: Kristen Perron

Additional Information

Data sheets and other additional information are available on [Analog Devices' web site](#)